AMENDMENT TO THE CLAIMS

The following is a detailed listing of all claims that are, or were, in the Application.

Claims 3 and 4 have been amended.

1. (Original) An integrated circuit die comprising:

functional circuitry;

a plurality of bond pads, each bond pad associated with a respective portion of the functional circuitry and for bonding the respective portion of the functional circuitry;

at least one probe pad for testing of the functional circuitry; and

multiplexing circuitry between the probe pad and the bond pads, the multiplexing circuitry for multiplexing signals between the probe pad and each of the respective portions of the functional circuitry, thus allowing the respective portions of functional circuitry to be tested using the probe pad and without any contact of the plurality of bond pads by a probe needle.

2. (Original) The integrated circuit die of Claim 1 wherein the multiplexing circuitry comprises a plurality of switching devices, each switching device coupled between the probe pad and a respective one of the bond pads.

3. (Amended) An integrated circuit die comprising:

functional circuitry;

a plurality of bond pads, each bond pad associated with a respective portion of the functional circuitry and for bonding the respective portion of the functional circuitry;

at least one probe pad for testing of the functional circuitry; ~~and~~

multiplexing circuitry between the probe pad and the bond pads, the multiplexing circuitry for multiplexing signals between the probe pad and each of the

respective portions of the functional circuitry, thus allowing the respective portions of functional circuitry to be tested using the probe pad and without any contact of the plurality of bond pads by a probe needle[.], and

a plurality of tri-state drivers for driving signals in the integrated circuit die, each tri-state driver coupled between a respective one of the bond pads and an associated portion of functional circuitry.

4. (Amended) An integrated circuit die comprising:

functional circuitry;

a plurality of bond pads, each bond pad associated with a respective portion of the functional circuitry and for bonding the respective portion of the functional circuitry;

at least one probe pad for testing of the functional circuitry; ~~and~~

multiplexing circuitry between the probe pad and the bond pads, the multiplexing circuitry for multiplexing signals between the probe pad and each of the respective portions of the functional circuitry, thus allowing the respective portions of functional circuitry to be tested using the probe pad and without any contact of the plurality of bond pads by a probe needle[.], and

a respective input/output buffer for each bond pad.

5. (Original) The integrated circuit die of Claim 1 wherein the functional circuitry comprises memory circuitry.

6. (Original) The integrated circuit die of Claim 1 wherein the functional circuitry comprises logic circuitry.

7. (Original) The integrated circuit die of Claim 1 wherein the probe pad is substantially the same size as each bond pad.

8. (Original) The integrated circuit die of Claim 1 wherein the probe pad is larger than each bond pad.

9. (Original) The integrated circuit die of Claim 1 wherein the distance between adjacent bond pads is about 50 microns or less.

10. (Original) The integrated circuit die of Claim 1 wherein the probe pad is provided along one edge of the integrated circuit die and the bond pads are provided at an opposing edge of the integrated circuit die.

11. (Original) A method of testing functional circuitry of an integrated circuit having a test pad and a plurality of bond pads, each bond pad associated with a respective portion of the functional circuitry and for bonding out the respective portions of the functional circuitry, the method comprising:

contacting the test pad with a probe needle; and

conveying a signal between the probe needle and at least one respective portion of the functional circuitry via the test pad, thus allowing the respective portions of functional circuitry to be tested using the test pad and without any contact of the plurality of bond pads by the probe needle.

12. (Original) The method of claim 11 wherein the signal is input from the probe needle to the integrated circuit die and further comprising demultiplexing the input signal into the portions of the functional circuitry.

13. (Original) The method of claim 11 wherein the signal is output from at least one portion of the functional circuitry and further comprising driving the signal out of the integrated circuit device.

14. (Original) The method of claim 11 wherein the signal is output from at least one portion of the functional circuitry and further comprising multiplexing the output signal.

15. (Original) The method of Claim 11 wherein the test pad is a bonding pad.

16. (Original) The method of Claim 11 wherein the test pad is a probe pad.

17. (Original) The method of Claim 11 wherein the test pad is located on the integrated circuit die remote from the bonding pads.

18. (Original) An integrated circuit die comprising:

functional circuitry;

a first plurality of bond pads positioned at a first edge of the integrated circuit die, each bond pad of the first plurality associated with a respective portion of the functional circuitry;

a second plurality of bond pads positioned at a second edge of the integrated circuit die; and

wherein at least one bond pad of the second plurality can be used for testing a portion of the functional circuitry associated with a bond pad of the first plurality.

19. (Original) The integrated circuit die of Claim 18 further comprising at least one multiplexer coupled to each of the bond pads of the first and second plurality.

20. (Original) The integrated circuit die of Claim 18 further comprising a buffer coupled between each bonding pad of the first plurality and the associated portion of the functional circuitry.

21. (Original) The integrated circuit die of Claim 19 further comprising a buffer coupled between the multiplexer and a bond pad of the either the first or second plurality.

22. (Original) The integrated circuit die of Claim 19 wherein the functional circuitry comprises memory circuitry.

23. (Original) The integrated circuit die of Claim 19 wherein the functional circuitry comprises logic circuitry.

24. (Original) A method of testing a plurality of integrated circuit dies arranged in rows on a wafer, each integrated circuit die having probe pads along one edge, the method comprising:

contacting the probe pads of integrated circuit dies on two rows of the wafer simultaneously with a plurality of probe needles of a probe arm; and

conveying respective signals between the probe needles and the contacted probe pads of the integrated circuit dies.

25. (Original) The method of claim 24 further comprising routing the signals from the probe pads to portions of the integrated circuit dies coupled to bond pads associated with the contacted probe pads.

26. (Original) The method of Claim 25 wherein routing comprises demultiplexing at least one of the signals and buffering at least one of the signals.

27. (Original) The method of Claim 25 wherein routing comprises closing at least one switch for the portions of the integrated circuit dies coupled to the bonding pads associated with the contacted probe pads while opening at least one switch for portions of

the integrated circuit dies coupled to the bonding pads associated with the remaining bonding pads.

28. (Original) An integrated circuit die comprising:

functional circuitry;

means for bonding wires to the functional circuitry;

means for applying one or more test signals to the functional circuitry, such that the means for bonding are not contacted by probe pins when the integrated circuit die is tested.

29. (Original) A method of testing a plurality of integrated circuit dies arranged in rows on a wafer, each integrated circuit die having probe pads along one edge, each probe pad switchably connected to a plurality of bonding pads of the respective integrated circuit die, the method comprising:

contacting the probe pads of integrated circuit dies on a first row and a second row of the wafer simultaneously with a plurality of probe needles of a probe arm; and

testing functional circuitry of at least one integrated circuit die on the first row and at least one integrated circuit die of the second row simultaneously.

30. (Original) The method of Claim 29 wherein the step of testing comprises:

closing a first switch associated with at least one of the plurality of bonding pads and opening at least a second switch associated with a remaining one of the plurality of bonding pads; and

sending a signal through one of the probe needles in contact with a probe pad.

31. (Original) The method of Claim 29 wherein the step of testing comprises multiplexing and demultiplexing a signal from the probe pads to the functional circuitry.

32. (Original) The method of Claim 30 further comprising buffering the signal.

33. (Original) A method of testing functional circuitry of an integrated circuit die comprising:

providing a probe pad on the integrated circuit die for a plurality of bonding pads, the probe pad for testing the functional circuitry, the bonding pads for bonding out respective portions of the functional circuitry; and

providing switching circuitry on the integrated circuit die for multiplexing signals between the probe pad and the respective portions of the functional circuitry, thereby allowing the respective portions of functional circuitry to be tested without any contact of the bonding pads by a probe needle.

34. (Original) The method of Claim 33 wherein the switching circuitry comprises a multiplexer.

35. (Original) The method of Claim 33 wherein the switching circuitry comprises a demultiplexer.

36. (Original) The method of Claim 33 wherein the probe pad is substantially the same size as each bonding pad.

37. (Original) The method of Claim 33 wherein the probe pad is larger than each bonding pad.

38. (Original) The method of Claim 33 wherein the probe pad is provided along one edge of the integrated circuit die and the bonding pads are provided at an opposing edge of the integrated circuit die.